CLAIMS

What is claimed is:

1. A method of erasing a flash electrically erasable programmable read only memory (EEPROM) device which includes a plurality of memory cells each having a charge storing layer including at least a first charge storing cell and a second charge storing cell, the charge storing layer being disposed between a top dielectric layer and a bottom dielectric layer, and a gate electrode disposed above the top dielectric layer, the bottom dielectric layer disposed above a substrate having a first conductive region adjacent the first charge storing cell and a second conductive region adjacent the second charge storing cell, said method comprising:

(a) applying an erase pulse to the plurality of memory cells;

(b) erase verifying the plurality of memory cells to determine if there are any undererased memory cells in the plurality of memory cells; and

(c) applying a positive gate stress to the plurality of memory cells to reduce the amount of positive charge within the charge storing layer.

2. The method according to claim 1, further comprising:

repeating steps (a) and (b) until all of the memory cells verify as not being undererased.

3. The method according to claim 2, further comprising:

preprogramming the plurality of memory cells to a predetermined level.

4. The method according to claim 2, wherein applying the positive gate stress is effective to correct any memory cells that are overerased.

5. The method according to claim 3, wherein step (c) includes:

grounding all bitlines coupled to at least one of the first and second conductive regions of each memory cell of the plurality of memory cells;

applying a positive voltage to all wordlines coupled to the gate electrodes of each memory cell of the plurality of memory cells.

6. The method according to claim 5, wherein the positive voltage applied to all of the wordlines is between about +9 volts and about +11 volts.

7. The method according to claim 6, wherein the positive voltage is applied as a voltage pulse having a duration of about 1 millisec (ms) to about 5 sec.

8. The method according to claim 1, further comprising:

applying a soft programming pulse to any memory cells in the plurality of memory cells which have a threshold voltage below a predefined minimum value.

9. The method according to claim 8, wherein applying a soft programming pulse includes:

applying a voltage potential of about +4 volts to about +8 volts to the gate electrode; and

applying a voltage potential of about +3 volts to about +5 volts to at least one of the first and second conductive regions.

10. The method according to claim 8, further comprising:

before the step of applying a soft programming pulse, soft program verifying the plurality of memory cells to determine whether any of the memory cells have a threshold voltage below the predefined minimum value.

11. The method according to claim 2, wherein step (a) includes:

applying a negative gate erase potential of between about -5 volts and about -10 volts to the gate electrodes of the plurality of memory cells, and

applying a voltage potential of between about +4 volts and about +8 volts to at least one of the first and second conductive regions of the plurality of memory cells.

12. A method to tighten a threshold voltage distribution curve in a memory device comprised of a plurality of memory cells each having a source and a drain disposed within a substrate, a bottom dielectric layer disposed above the substrate, a charge storing layer including a normal bit adjacent the drain and a complementary bit adjacent the source disposed above the bottom dielectric layer, a top dielectric layer disposed above the charge storing layer, and a gate electrode disposed above the top dielectric layer, wherein the memory cells are organized in rows and columns with the rows being wordlines and the columns being bitlines, the method comprising:

after an erase operation, applying a positive gate stress pulse to the gate electrode of each of the plurality of memory cells via the wordlines; and

grounding the source and the drain of each of the plurality of memory cells via the bitlines.

13. The method according to claim 12, wherein the positive gate stress pulse is about +8 volts to about +12 volts.

14. The method according to claim 13, wherein the positive gate stress pulse has a duration of about 1 millisec (ms) to about 5 sec.

15. The method according to claim 12, further comprising:

determining whether any of the plurality of memory cells has a threshold voltage below a predetermined minimum threshold voltage V_{TMIN}; and

applying a soft programming pulse to any memory cells having a threshold voltage below V_{TMIN}.

16. The method according to claim 15, wherein applying a soft programming pulse includes:

applying a voltage potential of about +4 volts to about +8 volts to the gate electrode of each memory cell having a threshold voltage below V_{TMIN}; and

applying a voltage potential of about +3 volts to about +5 volts to at least one of the source and the drain of each memory cell having a threshold voltage below V_{TMIN}.

17. The method according to claim 16, wherein the soft programming pulse has a duration of about 0.5 microsec (μs) to about 0.5 sec.

18. A flash electrically erasable programmable read only memory (EEPROM) device comprising:

a plurality of memory cells each having:

a source and a drain disposed within a substrate;

a bottom dielectric layer disposed above the substrate;

a charge storing layer including at least a first charge storing cell and a second charge storing cell disposed above the bottom dielectric layer;

a top dielectric layer disposed above the charge storing layer; and

a gate electrode disposed above the top dielectric layer;

wherein the memory cells are organized in rows and columns with the rows being wordlines coupled to the gate electrodes and the columns being bitlines coupled to the source and the drain; and

peripheral circuitry operative to apply voltage potentials to the wordlines and bitlines for performing erasure of the memory cells and applying a positive gate stress to the plurality of memory cells to correct any memory cells that are overerased.

19. The flash EEPROM device according to claim 18, wherein the peripheral circuitry is further operative to apply a positive gate stress voltage between about +8 volts and about +12 volts to all wordlines coupled to the gate

electrodes and to ground all bitlines coupled to at least one of the source and the drain.

20. The flash EEPROM device according to claim 19, wherein the peripheral circuitry is further operative to apply a soft programming pulse to any memory cells in the plurality of memory cells that have a threshold voltage below a predefined minimum value.